CLAIMS

What is claimed is:

1. A method of detecting variations in a spatially correlated parameter comprising:

measuring a selected parameter of each of a plurality of electronic circuits replicated on a common substrate;

calculating a difference between a value of the selected parameter at a target location and that of an identical relative location with respect to the target location for each of the plurality of electronic circuits to generate a distribution of differences;

calculating an absolute value of the distribution of differences; and

calculating an average of the absolute value of the distribution of differences to generate a representative value for the residual for the identical relative location.

2. The method of Claim 1 further comprising plotting the residual as a function of the identical relative location to determine a spatial correlation pattern of the selected parameter.

3. The method of Claim 1 wherein the electronic circuit is an integrated circuit die and the common substrate is a silicon wafer.

4. The method of Claim 1 wherein the selected parameter is quiescent current.

5. The method of Claim 1 further comprising performing a lot averaging for each wafer X-Y coordinate so that a new set of best estimates is re-calculated for each X-Y position.

6. The method of Claim 1 wherein the common substrate comprises a plurality of common substrates wherein best estimates for a given X-Y location are identical to those of a corresponding location on another of the plurality of common substrates. This technique may be improved by re-ordering the wafers in the sequence in which they were processed to ensure more accurate estimation.

7. The method of Claim 6 further comprising re-ordering the plurality of common substrates in a same order in which they were processed.

8. A process for reducing the variance of a selected parameter in a production lot of integrated circuits comprising:

measuring a selected parameter of each of a plurality of integrated circuit die replicated on a wafer substrate;

calculating a difference between a value of the selected parameter at a target location and that of an identical relative location with respect to the target location for each of the plurality of integrated circuit die to generate a distribution of differences;

calculating an absolute value of the distribution of differences;

calculating an average of the absolute value of the distribution of differences to generate a representative value for the residual for the identical relative location having an expected value range of the selected parameter at the identical relative location; and

rejecting any of the plurality of integrated circuit die having a value of the selected parameter that lies outside the expected value range.

9. The process of Claim 8 further comprising plotting the residual as a function of the identical relative location to determine a spatial correlation pattern of the selected parameter.

10. The process of Claim 8 wherein the selected parameter is quiescent current.